**ECE 374 Lab 8: Forwarding**

Due in Lab April 9, 2019

**Pre-Lab :** Extend the 5-stage pipelined processor from Lab 6&7 with two forwarding paths: MEM-to-EX and WB-to-EX. Figure 4.57 (page 312) shows the forwarding paths. Note that the ALUSrc MUX is placed in front of the second forwarding MUX. The logic for the forwarding unit is given in pages 308-311. The forwarding unit can be implemented as a separate VHDL component and then port-mapped into the top-level file. Rs and Rt register addresses need to be passed down the pipeline to the ID/EX pipeline registers as these values are required by the forwarding unit. The forwarding logic can be implemented using when/else VHDL statements (similar to the one used in the instruction decode unit). Test your design with code that has RAW hazards but that does not have load-use hazards. Since you have not implemented hazard detection logic, your pipeline cannot yet handle load-use hazards. Also, since you do not have a RAW register file, ensure that RAW hazards in your code will not require the use of a RAW register file to handle dependencies.

**Lab:** To be done in the lab (FPGA simulation). Show FPGA simulation to the TA for check off.